Digital Background Calibration for Capacitor Nonlinearity in Pipelined Analog to Digital Converter

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ABSTRACT: This paper presents a digital background calibration algorithm for 1.5bit/stage analog to digital converter. The error that discussed in this paper is: capacitor nonlinearity error due to MOSCAP of first stage of pipelined ADC. Proposed calibration algorithm uses an 16 bit sigma-delta ADC for calibration and coefficient is updated with LMS algorithm. A 14-bit pipelined ADC is simulated by Matlab Simulink. After calibration, simulation gives a great improvement in SNDR and SFDR.

Keywords: Background calibration, LMS algorithm, Nonlinearity, Pipelined ADC.

INTRODUCTION

An analog-to-digital converter get an input voltage from analog domain and converts it to a digital code. For a N-bit pipelined ADC, after normalization of input voltage to a reference voltage, the output of converter (D) will be:

\[ D_{out} = D_1 2^{N-1} + D_2 2^{N-2} + ... + D_N = \sum_{i=0}^{N} D_i 2^{-i} = x + e_q \text{ with } |e_q| \leq 2^{-N} \]  

Where \( d_k \) is \((-1,0,1)\) for 1.5 bit/stage, \( x \) is normalized input and \( e_q \) is quantization error (Keane, 2005). The linearity of pipeline ADC is reduced by reduction in linearity of it’s analog circuit. The source of linearity errors in pipelined ADC are: linear gain error in residue amplifier due to finite gain of operational amplifier and nonlinearity of capacitor-mismatch errors in sub-DAC (Taherzade-Sani, 2010). But by using nonideal capacitor, linear error of capacitor-mismatch will changed to nonlinear error.

The calibration schemes can be divided into two major kinds: analog and digital calibration. By using analog calibration, the maximum effective number of bit (ENOB) will be 8 to 10 bits. Another scheme is digital calibration that is divided to foreground and background calibration. Foreground calibration interrupted the operation of ADC and is not suitable for all applications, particularly in systems that interruption is not allowed. Another kind of digital calibration is background calibration. The digital background calibration is most popular than other kinds, because of no need for interruption and down scaling of circuit implementation with the layout development (Kaihui, 2009). Digital background calibration divide into three schemes: the first scheme uses an extra ADC which is a high resolution but low speed ADC, like sigma-delta (Tsang, 2008). The second scheme is static-based calibration (Murmann, 2003), and third one is dither-based algorithm, (Meruva, 2007). In this paper first one is used for calibration of pipelined ADC. The error discussed in this paper is capacitor nonlinearity.

Modelling of MOSCAP behaviour in 1.5-bit/stage pipelined ADC is presented in section 2. Section 3 presents digital background calibration by using sigma-delta ADC. Section 4 is simulation results. Section 5 concludes this paper.

Modeling of MOSCAP Behaviour in 1.5-Bit Pipelined ADC

As shown in Fig. 1, each pipeline ADC is composed of a sub-ADC and sub-multiplying DAC, called MDAC. MDAC is consist of sample and hold circuit, sub-DAC and an adder. Errors in sub-blocks cause reduction in resolution of the converter. Modelling of flip-around implementation is shown in Fig. 2. In ideal circuit the output of each stage is given by:

\[ V_o = (1 + \frac{C}{C_f}) Vin - D \frac{C}{C_f} \]  

(2)
Where D is -1,0, 1, C_s is sampling capacitor and C_f is flip-around capacitor. Ø1 is for sampling phase and Ø2 is for evaluation phase.

Figure 1. Block diagram of Pipelined ADC

Figure 1. Flip-around model of Pipelined ADC

At sampling phase, both C_s and C_f are connected to Vin. At evaluation phase flip-around capacitor is connected to the output and sampling capacitor connected to the output of sub-DAC.

By modelling capacitors with nonideal capacitors, the output will change and some error appears in the output. One of this nonideal models is MOSCAP, that discussed in (Aminzadeh, 2007). As shown in (Aminzadeh, 2007), the model of this capacitors follow from Eq. (3)

\[ C_s = C_{s0} \left(1 + mv_s^2\right); \quad C_f = C_{f0} \left(1 + mv_f^2\right) \]  \hspace{1cm} (3)

Where \( C_{s0} \) and \( C_{f0} \) are constant values of capacitors and m is related to type of technology.

In sampling phase the stored charge on two capacitors is

\[ Q_s = \int_{0}^{V_o} (C_{s0} + C_{s0})(1 + mv_s^2)dv \]  \hspace{1cm} (4)

And in evaluation phase, stored charge is

\[ Q_f = \int_{0}^{V_o} (C_{s0})(1 + mv_s^2)dv + \int_{0}^{V_o} C_{f0} \left(1 + mv_f^2\right)dv \]  \hspace{1cm} (5)

From (4) equals to (5), it is concluded (6):

\[ Q_f = \int_{0}^{V_o} (C_{s0})(1 + mv_s^2)dv + \int_{0}^{V_o} C_{f0} \left(1 + mv_f^2\right)dvV_o + \frac{1}{3}mV_o^3 = \left(1 + \frac{C_{s0}}{C_{f0}}\right)(V_o + \frac{1}{3}mV_o^3) - D \frac{C_{s0}}{C_{f0}} \left(1 + \frac{1}{3}V_{ref}^3\right) \]  \hspace{1cm} (6)

If \( C_{s0} \) is equal to \( C_{f0} \) the equation changed to (7)
Calibration of Capacitor Error By Using LMS Algorithm

One of Calibration methods is LMS algorithm. This algorithm is shown in Fig. 3. As shown in this figure, by using an extra ADC the error between real and ideal ADC is detected, then by using Eq. (8) the error coefficient is updated.

$$W'(t+1) = W'(t) + \mu \cdot U(t) \cdot e(t)$$  \hspace{1cm} (8)

Where $W$ is the error coefficient matrix and it is updated by using error at output and $\mu$ is convergence constant of LMS algorithm, $U$ and $e$ are input and error of output, respectively.

RESULTS

Simulation Results

In this paper a 14-bit, 1.5bit/stage, 50 Msps pipeline ADC is simulated with Matlab Simulink. Since the first stage of converter is very important in conversion result, error is injected to first stage of converter. The mismatch of capacitor, assumed to be 6% ($m=0.06$). The error coefficient is initialized to it’s ideal value, that is zero. $\mu_m$ is selected to $2^{-12}$. Fig. 4 and 5 show output spectrum before and after calibration. A significant improvement in dynamic characteristics after calibration is obtained. The equation for calculation of ENOB is

$$ENOB = SNDR - 1.76) / 6.02$$  \hspace{1cm} (9)

Table 1 compares the results before and after calibration.

<table>
<thead>
<tr>
<th></th>
<th>Before calibration</th>
<th>After calibration</th>
</tr>
</thead>
<tbody>
<tr>
<td>SFDR</td>
<td>40.2</td>
<td>77.4</td>
</tr>
<tr>
<td>SNR</td>
<td>56.82</td>
<td>75.8</td>
</tr>
</tbody>
</table>

CONCLUSION

A digital background calibration based on LMS algorithm was proposed for estimation and calibration of capacitor mismatch nonlinearity of first stage of pipeline ADC. The proposed algorithm was implemented in 14-bit 1.5bit pipeline ADC. Simulation results showed significant improvement in characteristics of converter. Calibration of both gain error and capacitor nonlinearity, is proposed for future works.
Figure 3. a) PSD before calibration, b) PSD after calibration

REFERENCES


